AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

Claims 1-10. (Canceled).

11. (New) An LSI comprising:

a central processing unit; and

a memory controller for controlling an external memory,

wherein said memory controller is operable to receive a request for access from said central processing unit to said external memory having a data storage area divided into a plurality of banks each divided into a plurality of pages, and

wherein said memory controller is operable to activate a page of said external memory to be accessed, based on said access request from said central processing unit, and to execute advance precharge of a page to be accessed subsequently by said central processing unit before accessing said activated page.

12. (New) An LSI according to claim 11,

wherein data of said central processing unit is stored in said external memory.

13. (New) An LSI according to claim 12,

wherein said memory controller is operable to provide a RAS signal, a CAS signal, a WE signal and an address signal to said external memory synchronized with a clock signal.

14. (New) An LSI according to claim 12,

wherein said memory controller is operable to provide a bank address signal and an address signal to said external memory synchronized with a clock signal.

15. (New) An LSI for processing comprising:

a central processing unit to execute data processing; and

a memory control unit operable to read access or write access to an external DRAM,

wherein said memory control unit is operable to receive a request for access from said central processing unit to said external DRAM having a data storage area divided into a plurality of banks each divided into a plurality of pages; and

wherein said memory control unit is operable to activate a page of said external DRAM to be accessed, based on said access request from said central processing unit, and to execute advance precharge of a bank next to be accessed by said central processing unit before accessing said activated page.

16. (New) An LSI for processing according to claim 15,

wherein said memory control unit is operable to provide a RAS signal, a CAS signal, a WE signal and a bank address signal to said external memory synchronized with a clock signal.

17. (New) An LSI for processing according to claim 15,

wherein said central processing unit is operable to access for read out an instruction code stored in said external memory.

18. (New) An LSI for processing according to claim 17,

wherein said memory control unit is operable to provide a bank address signal and an address signal to said external DRRAM synchronized with clock signals.

19. (New) An LSI comprising:

a CPU to execute data processing; and

a memory controller to access to an external memory synchronized with clock signals,

wherein said memory controller is operable to receive a request for access from said CPU to said external memory having a data storage area divided into a plurality of banks each divided into a plurality of pages, each page being allocated to a bank different from banks to which pages adjacent to said page are allocated, and

wherein said memory is operable to activate a page of a bank to be accessed, based on said access request from said CPU, and to execute advance precharge of a page of the bank to be accessed subsequently by said CPU before accessing said activate page.

20. (New) An LSI according to claim 19,

wherein data of said CPU is stored in said external memory.

21. (New) An LSI according to claim 20,

wherein said memory controller is operable to provide a RAS signal, a CAS signal, a WE signal and bank address signal to said external memory synchronized with said clock signals.

22. (New) An LSI according to claim 19,

wherein said memory controller is operable to provide a bank address signal and an address signal to said external memory synchronized with said clock signals.